IN THE CLAIMS

1. (Currently Amended) An apparatus, comprising:

an interface for directly coupling to a host bus having one or more processors without being shared with a host-to-PCI bridge;

a device coupled to the interface to perform one or more functions, said device appearing as a virtual PCI device~~, other than a virtual host-to-PCI bridge,~~ logically residing on a PCI bus that is coupled to the host bus through [[a]] the host-to-PCI bridge, wherein access by the device to the host-to-PCI bridge is only through the host bus; and

a monitor circuit coupled to said interface and said device to track host bus cycles initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to the virtual PCI device, and to generate one or more control signals to enable the device to respond, as the virtual PCI device, to said one or more of said identified host bus cycles targeted to said virtual PCI device without having to access the host-to-PCI bridge.

2. (Currently Amended) The apparatus of claim 1, further comprising a first storage coupled to the interface and the monitor circuit to store data associated with host bus read cycles addressed to the virtual PCI device, wherein the data is transferred from the first storage to the host bus during the host bus read cycles without accessing a host interface of the host-to-PCI bridge.

3. (Currently Amended) The apparatus of claim 2, further comprising a second storage coupled to the interface and the monitor circuit to store data associated with host bus write cycles addressed to the virtual PCI device, wherein the data is transferred from the host bus to the second storage during the host bus write cycles without accessing the host interface of the host-to-PCI bridge.

4. (Currently Amended) The apparatus of claim 1, further comprising a processor coupled to the interface, the processor capable of initiating one or more host bus cycles on the host bus via the interface ~~which is coupled to said host bus, wherein said processor, said first storage, and said monitor circuit are integrated into a single chip package~~.

5. (Previously Presented) The apparatus of claim 3, further comprising an internal bus to connect the device, the monitor circuit, and the first and second storages to the interface.

6. (Previously Presented) The apparatus of claim 1, wherein the device is a bridge device coupled to one or more other devices and the device appears as a virtual PCI-PCI bridge logically residing on a PCI bus coupling to the host-to-PCI bridge.

7. (Previously Presented) The apparatus of claim 1, wherein said identified host bus cycles targeted to said virtual PCI device include host bus cycles targeted to memory address space allocated to said virtual PCI device.

8. (Original) The apparatus of claim 1, further comprising a mirror register coupled to said host bus and responsive to one or more of said control signals to receive data from said host bus;

wherein said monitor circuit is to further identify host bus write cycles targeted to a configuration-address register; and

wherein said monitor circuit is to generate said control signals to receive data from said host bus to store in said mirror register during said host bus cycles identified as targeted to said configuration-address register.

9. (Previously Presented) The apparatus of claim 1, wherein said identified host bus cycles targeted to said virtual PCI device include host bus cycles to I/O address space allocated to said virtual PCI device.

10. (Previously Presented) The apparatus of claim 2, wherein said first storage includes a first plurality of configuration registers; and

wherein said identified host bus cycles include host bus cycles targeted to configuration space reserved for said virtual PCI device.

11. (Currently Amended) The apparatus of claim 10, wherein said virtual PCI device resides behind a virtual PCI-to-PCI bridge, ~~and~~ wherein said first storage includes a second plurality of configuration registers, and wherein said monitor circuit is to further identify host bus cycles targeted to configuration space allocated to said virtual PCI-to-PCI bridge, and wherein said monitor circuit is to generate said plurality of control signals to transfer ~~a select~~

one or more said data to said host bus during one or more of said identified host bus read cycles targeted to said configuration space allocated to said virtual PCI-to-PCI bridge.

12. (Currently Amended) An apparatus, comprising:

an interface for directly coupling to a host bus without being shared with a host-to-PCI bridge;

a first storage, wherein contents of said first storage specify a first address space allocated to a primary PCI bus;

a device coupled to the interface to perform one or more functions, the device appearing as a virtual PCI device~~, other than a virtual host-to-PCI bridge,~~ logically residing on a PCI bus coupled to the primary PCI bus, wherein access by the device to the host-to-PCI bridge is only through the host bus;

a second storage, wherein contents of said second storage specify a second address space allocated to said virtual PCI device; and

a control circuit, coupled to said first and said second storage, wherein said control circuit is to couple to a host bus to track processor initiated host bus cycles and to select host bus cycles to route to said primary PCI bus, wherein said routed cycles are to be selected, based on said contents of said first storage and said second storage, to exclude host bus cycles targeted to said second address space.

13. (Original) The apparatus of claim 12, wherein said first and said second address space includes memory host bus address space.

14. (Original) The apparatus of claim 12, wherein said first and said second address space includes host bus I/O space.

15. (Original) The apparatus of claim 12, wherein said first and said second address space includes PCI compliant configuration address space.

16. (Original) The apparatus of claim 12, wherein said virtual PCI device is a virtual PCI-to-PCI bridge.

17. (Currently Amended) The apparatus of claim 16, further comprising:

a plurality of configuration registers;

a third storage coupled to said control circuit, wherein contents of said third storage indicate a bus and a device number in which said virtual PCI-to-PCI bridge logically resides, and wherein said control circuit is to further select, based on said bus and said device number, host bus cycles, targeted to configuration address space of said virtual PCI-to-PCI bridge, to route to said plurality of configuration registers without having to access a host interface of the host-to-PCI bridge.

18. (Currently Amended) A system comprising:

one or more processors coupled to a host bus;

a host-to-PCI bridge coupling a primary PCI bus to the host bus, said host-to-PCI bridge to route ~~select~~ processor initiated host bus cycles to the primary PCI bus; and

a first host bus device coupled to said host bus and appearing as a first virtual PCI device~~, other than a host-to-PCI bridge,~~ logically residing on a PCI bus coupled to the primary PCI bus, to monitor said host bus, to identify processor initiated host bus cycles targeted to said first virtual PCI device, and to intercept ~~select~~ said identified cycles targeted to said first virtual PCI device without accessing the host-to-PCI bridge, wherein access by the device to the host-to-PCI bridge is only through the host bus;

wherein said host-to-PCI bridge does not forward said identified cycles to the PCI bus coupled ~~to~~ via the host-to-PCI bridge, which are targeted to said first virtual PCI device.

19. (Original) The system of claim 18, wherein said first host bus device includes a plurality of configuration registers, wherein said intercepted cycles, include host bus cycles targeted to configuration space reserved for said first virtual PCI device and are to be routed to access said plurality of configuration registers.

20. (Previously Presented) The system of claim 18, wherein said first host bus device includes an array of memory devices, wherein said intercepted cycles include host bus cycles targeted to a memory space allocated to said first virtual PCI device and are to be routed to access said array of memory devices.

21. (Previously Presented) The system of claim 18, further comprising a second host bus device coupled to said host bus, the second host bus device appearing as a second virtual PCI device logically residing on a PCI bus coupled to the primary PCI bus, and the first and

second virtual PCI devices having a unique combination of a PCI bus number and device number.

22. (Previously Presented) The system of claim 18, wherein said first virtual PCI device resides logically behind a primary virtual PCI-to PCI bridge, wherein said primary virtual PCI-to-PCI bridge resides logically behind said primary PCI bus, and wherein said first host bus device is to snoop said host bus to determine a bus number assigned to said primary virtual PCI-to PCI bus.

23. (Previously Presented) The system of claim 22, wherein said first virtual PCI device resides logically behind a secondary virtual PCI-to PCI bridge which resides logically behind said primary virtual PCI-to-PCI bridge,

wherein said first host bus device includes a plurality of bridge configuration registers, and wherein said intercepted cycles include host bus cycles targeted to the configuration space reserved for said secondary virtual PCI-to PCI bridge and are to be routed to access said plurality of bridge configuration registers.

24. (Currently Amended) A method comprising:

capturing a current host bus cycle initiated by a processor coupled to a host bus;

determining whether said captured cycle is targeted to a virtual PCI device~~, other than a virtual host-to-PCI bridge,~~ residing logically at a PCI bus behind a primary PCI bus, the virtual PCI device representing a host bus device directly coupled to the host bus without having to share an interface with a host-to-PCI bridge

and without having to access a host interface of the host-to-PCI bridge in order to access the host bus;

intercepting said current host bus cycle, if said current cycle is determined to be targeted to said virtual PCI device, without routing said cycle to said primary PCI bus via the host interface of the host-to-PCI bridge; and

routing the intercepted host bus cycle to the host bus device without using the host interface of the host-to-PCI bridge to enable the host bus device to respond, as said virtual PCI device, to the host bus cycle.

25. (Original) The method of claim 24, wherein said intercepting includes routing to access a storage coupled to said host bus.

26. (Original) The method of claim 24, wherein said intercepting includes routing to access a location within a plurality of configuration registers.

27. (Original) The method of claim 24, wherein said determining includes determining whether said current cycle is a write cycle targeted to a configuration-address register and snooping said current host bus cycle to receive data from said host bus if said current cycle is a write cycle targeted to said configuration-address register and writing some or all of said data into a mirror register.

28. (Original) The methods of claim 24, wherein said determining includes determining whether said current cycle is a write cycle targeted to a location within the configuration registers of a virtual primary PCI-to-PCI bridge in which a bus number is specified; and

snooping said current host bus cycle to receive data from said host bus if the current cycle is a write cycle to a location within the configuration registers of a virtual primary PCI-to-PCI bridge in which a bus number is specified and writing said data in a storage.

29. (Original) The method of claim 24, wherein said determining includes determining whether said cycle is to a location within the configuration registers of a virtual PCI-to-PCI bridge; and

intercepting said current host bus to route to access a location within a plurality of bridge configuration registers if said cycle is to a location within the configuration registers of a virtual PCI-to-PCI bridge.

30. (Original) The method of claim 24 wherein said virtual PCI device is a virtual PCI-to-PCI bridge.